ods. Openings are formed in dielectric layer **106** and one or more conductive materials (e.g., metal, silicide, etc.) are deposited and patterned to produce the structure shown in FIG. **5**F. In this cross-sectional view, source electrode **109** provides electrical connection to N+ source region **105**, and electrodes **110***a* and **110***b* provide electrical connection to field plate members **103***a* and **103***b*, respectively.

FIG. **5**G shows the device structure of FIG. **5**F following formation of a drain electrode **111** on the bottom of N+ substrate **100**. For example, drain electrode **111** may be formed using the conventional technique of metal sputtering. As described earlier, the bottom of the substrate may first be subjected to grinding, implanting, etc., to lower the drain contact resistance.

The device of FIG. **5**G represents a completed high-voltage transistor having a stand-alone drift region; that is, the device of FIG. **5**G does not include a low-voltage, series MOSFET structure at the top of the epitaxial layer. Instead, the extended drift region formed by the epitaxial layer, itself, performs the function of the MOSFET without the inclusion of a P-body region. Practitioners in the arts will note that in this device structure current cannot be completely turned-off, since there exists a continuous n-type path for electrons to flow from source electrode **109** to drain electrode **111**. Current flow in the device structure of FIG. **5**G, however, does saturate when the mesa-like epitaxial layer **101** is pinched-off at high drain voltages.

The device structure of FIG. **6** achieves pinch-off of the extended drain region at lower voltages than the device of FIG. **5**G. This is achieved by reducing the spacing between the field plate members **103** and epitaxial layer **101** near the top of the N-type drift region, thereby increasing the capacitance to pinch-off the vertical drift region at a relatively low voltage. FIG. **6** shows a multi-tiered field plate structure extending laterally into oxide regions **102***a* & **102***b* to control the pinch-off voltage and, therefore, the saturation current. Alternatively, the field plate members may comprise a single step, a linearly graded lateral extension, or some other profile shape designed to achieve the same result.

Those skilled in the arts will appreciated that for certain circuit applications it may be advantageous to utilize the stand-alone transistor structure of FIG. **5**G (or FIG. **6**) in series with an ordinary external, low-voltage switching MOSFET. In such an application the low-voltage (e.g., 40V) MOSFET could be used for switching purposes in order to completely turn off current flow in the high-voltage (e.g., 700V) transistor device.

Referring now to FIGS. **5**H–**5**K, there is shown an alternative processing sequence that may be used to fabricate a vertical HVNMOS transistor that includes an insulated gate MOS structure.

Trenches **112***a* and **112***b* are formed in respective dielectric layers **102***a* and **102***b* on opposite sides of epitaxial layer **101** to accommodate the formation of the insulated gate structure. The depth of trenches **112***a* and **112***b* extends from the surface of epitaxial layer **101** to a depth governed by the intended MOSFET channel length and field plating considerations. In this example, the trench depth is about 1–5 um. By way of example, trenches **112** may be formed by appropriate application of a patterned masking layer to the semiconductor substrate followed by conventional dry or wet etching techniques into oxide layer **102**.

FIG. **5**I shows the device after formation of gate dielectric layers **116** and gate members **113** within trenches **112**. The gate dielectric layers **116***a* & **116***b* may be formed by growing or depositing oxide on the sidewalls of the exposed epitaxial layer **101**. The device threshold voltage and other device performance targets determine the thickness of layers **116**. In one embodiment, layers **116** comprise silicon dioxide having a thickness on the order of 250–1000 angstroms.

In the embodiment shown, a portion of dielectric layer **102** isolates field plate members **103** from gate members **113**. Alternatively, trenches **112** may expose the top portion of field plate **103** and the same processing steps used to create layers **116** may also be used to form dielectric layers on the sidewalls of the field plates to isolate the field plates from the gate members.

Once dielectric layers **116** have been formed on the sidewalls of trenches **112**, a conductive material, such as doped polysilicon, may be deposited to fill the remaining portions of the trenches. In this implementation, the doped polysilicon forms the gate members **113***a* and **113***b* of the MOS transistor structure. In the embodiment of FIG. **51**, the surface has been planarized using conventional etch-back and/or CMP techniques.

FIG. **5**J shows the device after introduction of a P-body region **107** and a N+ source region **105** at the top surface of epitaxial region **101**. Regions **107** and **105** may be formed using standard implantation, deposition, and/or thermal diffusion processing steps. In the completed device, application of a sufficient voltage to gate members **113** causes a conductive channel to be formed along the sidewall portions of P-body region **107** between N+ source region **105** and epitaxial region **101**. The channel length is therefore determined by the depth of P-body region **107**, and N+ source region **105**. For the particular embodiment shown the former may be approximately 0.5 um–3.0 um, and the latter in the range of about 0.1–0.5 um. A shorter channel length results in a lower channel resistance, which likewise reduces the on-resistance of the device. It should be understood, however, that a too short channel would cause punch-through problems. In other embodiments, the P-body and/or N+ source may be formed earlier in the process, for example before the trench etching of the epitaxial layer **101**, or before the trench etching of the oxide layer **102**.

FIG. **5**K shows the completed HVFET device structure following formation of an interlevel dielectric layer **106** (e.g., silicon dioxide, silicon nitride, etc.). This layer may be deposited and patterned to form contact openings. In the embodiment shown, the etching of layer **106** is followed by etching of the field plates, gate members, N+ and P-body regions. This is followed by deposition and patterning of one or more conductive layers (e.g., metal, silicide, etc.) to create source electrode **109**, gate electrodes **115**, and field plate electrodes **110**, which provide electrical connection to the respective regions of the device. The optional etching step described above allows the source electrode to contact the P-body region without patterning the N+ source region, thus simplifying the process. An additional P-type doping process may also be included for improved contact to the P-body. A conductive layer may also be applied to the bottom of substrate **100** (after optional treatment by grinding, etching, implanting, etc.) to form the drain electrode **111**.

Note that while source electrode **109** is shown extending down to P-body **107** in the cross-sectional view of FIG. **5**K, in other embodiments electrode may only extend to the upper surface of source region **105**.

We claim:

1. A high-voltage transistor comprising:

a drain region of a first conductivity type;

a source region of the first conductivity type;